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CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications

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About the Authors

Paul Muller received the engineering degree (diploma) in electrical engineering from the École Polytechnique Fédérale de Lausanne (EPFL) in 1999. From 1999 to 2002, he worked as a mixed-signal design engineer at XEMICS (now part of Semtech Corp.), where he contributed to several sensing and data-acquisition circuit designs. In 2002, he joined the Microelectronic Systems Laboratory (LSM) at EPFL as a research assistant, where he obtained his Dr. Sc. degree in electrical engineering in July 2006. His thesis research was on the modeling and design of multichannel gigabit receivers for short-distance optical communication interfaces, including design, modeling and test of transimpedance amplifiers, limiting amplifiers and clock and data recovery circuits. Since 2006, he is with Marvell Switzerland Sàrl., a subsidiary of Marvell Technology Group Ltd. He has published a number of papers in international conferences in the field and is a member of the IEEE.

Yusuf Leblebici received the B.S. and M.S. degrees in electrical engineering from Istanbul Technical University (ITU) in 1984 and 1986, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1990. Between 1991 and 2001, he worked as a faculty member at the University of Illinois at Urbana-Champaign, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI) in Massachusetts. From 2000 to 2001, he took the responsibility of developing the microelectronics degree program at Sabanci University, while also continuing his academic involvement at WPI during this time, as an affiliate associate professor. Since January 2002, Dr. Leblebici is a full (chair) professor at the École Polytechnique Fédérale de Lausanne (EPFL) and director of the Microelectronic Systems Laboratory.

Dr. Leblebici is the author or coauthor of more than 150 scientific articles published in international journals and conferences, and two textbooks. He has served on the organizing and steering committees of several international conferences in the field of integrated circuits. He is a senior member of the IEEE, served as associate editor of IEEE Transactions on Circuits and Systems II and associate editor of IEEE Transactions on VLSI.

Foreword

The intention of this book is to address a number of timely, performance-critical issues within the field of short-distance optical communications, from a circuit designer's perspective. It discusses the major trade-offs the designer has to deal with in the development of monolithically integrated receivers in CMOS technologies. As such, it is based on Dr. Muller's doctoral dissertation entitled "A Standard CMOS Multi-Channel Single-Chip Receiver for Multi-Gigabit Optical Data Communications", submitted to the School of Engineering of the École Polytechnique Fédérale de Lausanne (EPFL) in May 2006. The dissertation material has been enhanced by the presentation of a number of alternative design approaches and circuit topologies, providing exhaustive coverage of the state of the art in optical short-distance receiver circuit design.

The need for a new processor input/output (I/O) interface paradigm is dictated by ongoing technology scaling and the advent of multi-core systems. Indeed, each new generation of microprocessors and digital signal processors provides higher computing power and data throughput, whereas the available bandwidth of the I/O interfaces is subject to much slower growth. Moving beyond upcoming serial links to an optical data link paradigm for very short-distance (board-to-board and chip-to-chip communications allows for considerable I/O interface bandwidth enhancement. Fully integrated silicon CMOS receivers are considered to be the technology of choice to lead this solution to economic success, because monolithic integration results in lower volume-manufacturing cost, improved yield and reduced assembly and test expenses.

This book provides the reader with the necessary background knowledge to fully understand the trade-offs in optical short-distance communication receiver design. Thorough discussion of the presented material guides the reader in his design choices and leads to in-depth understanding of the design

trade-offs he is facing. An exhaustive list of references and suggestions for further reading complement the technical material presented in the book.

With its timely and up-to-date content, this book could be categorized as required reading for practicing engineers and researchers in the field of short-distance optical communications and optical CMOS receiver design, as well as for graduate students and photonics engineers working on high-speed photodetection systems.

This book would not have taken shape without the input and feedback of many people, which directly or indirectly influenced the research on which it is based. We are indebted to Professor M. Selim Ünlü and Dr. Matthew Emsley from Boston University, who laid the foundations of this project with their work on resonant cavity enhanced photodetectors. Particular thanks go to Dr. Armin Tajalli from the École Polytechnique Fédérale de Lausanne (EPFL) for his contribution to the clock recovery analysis and design. We would also like to express our profound gratitude to Dr. Thomas Morf and Dr. Martin Schmatz, from IBM Zurich Research Laboratory for their very valuable and regular feedback on this work, as well as Mr. Larry DeVito from Analog Devices for the tremendous review of the dissertation manuscript. We greatly appreciated the collaboration and discussion with the staff of IBM Research in Zurich, researchers from the École Centrale de Lyon and fellow researchers from the École Polytechnique Fédérale de Lausanne.

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Paul Muller

Etoy, May 2007

Yusuf Leblebici

Lausanne, May 2007

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Constants, Symbols and Acronyms

Constants

Symbol	Description	Value
ε_0	Permittivity of free space	$8.8542\ 10^{-12}$ F/m
μ_0	Permeability of free space	$0.4\pi\ 10^{-6}$ H/m
h	Planck constant	$6.626\ 10^{-34}$ Js
k_B	Boltzmann constant	$1.3806\ 10^{-23}$ J/K
q	Electron charge	$1eV = 1.6022\ 10^{-19}$ C

List of Symbols

Symbol	Description	Units
β	Transconductance parameter in bulk-referenced model	A/V^2
β	Amplifier feedback coefficient in TIA configuration	–
β_{BB}	BB path gain in higher-order BB loop	–
β_{int}	Integral path gain in higher-order BB loop	–
Δf_{TR}	CDR frequency tuning range	MHz or GHz
γ	Excess thermal noise factor	–
η	Quantum efficiency	–
f_0	Channel surface potential	V
ϕ_e	Phase error	rad
ϕ_F	Fermi potential in the the substrate	V
ϕ_i	Phase of the input (data) signal	rad

ϕ_o	Phase of the output (recovered clock) signal	rad
κ	Oscillator noise parameter	–
q	Time-varying phase angle	rad
μ_e	Electron mobility	$cm^2/(Vs)$
ρ_{PD}	Phototdetector responsivity	A/W
σ_0	RMS noise amplitude on logic “0”	V
σ_1	RMS noise amplitude on logic “1”	V
σ_{CKJ}	RMS oscillator clock jitter amplitude	UI
σ_{RJ}	RMS random jitter amplitude	UI
$\tau_{transit}$	PD transit time constant	μs
υ	Optical frequency	nm
ξ	Body-effect factor in source-referenced model	–
ζ	ISI proportionality factor	–
ζ	Transfer function damping factor	–
ω_n	Transfer function natural frequency	rad/s
ω_{pi}	Open-loop bandwidth of a single LA stage	rad/s
ω_{TIA}	TIA open-loop bandwidth	rad/s
A_{vi}	Voltage gain of a single LA stage	dB
A_{vDC}	Limiting amplifier DC voltage gain	dB
A_{vDCi}	DC voltage gain of a single LA stage	dB
A_{vLA}	Limiting amplifier voltage gain	dB
A_{vOS}	Offset compensation voltage gain in LA	dB
A_{vTIA}	TIA core amplifier voltage gain	dB
A^0_{vTIA}	TIA core amplifier open-loop DC gain	dB
BER	Bit error ratio	–
BW_{LA}	Limiting amplifier bandwidth	GHz
BW_{TIA}	Transimpedance amplifier closed-loop bandwidth	GHz
C_c	AC-coupling capacitance	fF
C_d	Drain junction capacitance	fF
C_f	TIA feedback capacitance	fF
C_{gs}	Gate-source capacitance	fF
C_{inCDR}	CDR input capacitance	fF
C_{inLA}	Limiting amplifier input capacitance	fF
C_L	Load capacitance	fF
C_{PD}	Photodetector capacitance	fF