Chapter 2

FAULT AND FAULT MODELLING

2.1 Introduction

The rise of system-on-chip (SOC) technology has dramatically boosted the importance of analog circuitry, moving it more into mainstream integrated circuit (IC) design. Analog and digital circuits are now being integrated into a SOC. Advances in deep sub-micron technologies has fuelled the explosive increase in IC complexity. The smaller size makes these chips more sensitive to fabrication variations and tolerance accumulations. Thus there is a growing demand for fault tolerance, which can be achieved not only by improving the reliability of the functional units, but also by an efficient fault detection, isolation and accommodation concept. Consequently, testing and fault diagnosis is becoming one of the major cost factors in the overall IC manufacturing expenses. It has been recognised as a valuable means to (a) check system installation and configuration after maintenance activities, (b) ensure correct system functionality at start-up, and (c) avoid masking and accumulation of errors during operation. Availability of a system (or of redundant system components) can be significantly increased, if testing is employed to allow rapid diagnosis after a failure.

In the context of fault diagnosis, a fault is understood as any kind of malfunction in the system that leads to an unacceptable anomaly in the overall system performance. A fault in a system can be very costly in terms of loss of production, equipment damage and economic setback. Faults are developed in a system due to normal wear and tear, design or manufacturing defects or improper operation leading to stress beyond endurable limits. In many cases degradation in the performance of the system is sustained for some duration before it actually “fails”. In many other cases a system

continues to operate with a failed component resulting in degraded performance.

The variety of fault modes that can occur may be classified as:

1. Abrupt (sudden) faults, i.e., step-like changes.
2. Incipient (slowly developing) faults, e.g., drift or bias.

Typically, abrupt faults play an important role in safety-critical applications (e.g. in power plants, transportation systems and drug manufacturing systems, etc,), where a system failure have to be detected early enough so that disastrous consequences arising due to failures can be avoided by early system reconfiguration. On the other hand, incipient faults are of major relevance in connection with maintenance problems where early detection of worn out components is required. In this case faults are typically small and not as easy to detect, but the detection time is of minor importance and may therefore be large.

In the study of fault diagnosis the construction of a fault dictionary using fault simulation techniques are widely used for choosing the test strategy. Some methodologies use schematics as the starting point to generate fault lists in fault simulation. For example, when a fault list is generated, every component is either shorted, or opened, shorted to power, shorted to ground in single fault situation, or a large number of different fault combinations are considered in multiple fault cases. The disadvantage of doing so is that it neglects the physical layout information of the circuitry and hence it could generate some unrealistic faults in the lists or a prohibitively large fault list. Therefore very often a single fault assumption is made. Unfortunately such assumption is often invalid. For instance, a single cut line across a PCB generates multiple faults. One problem in schematic based fault generation without layout information is its inaccuracy in fault models. For example, in CMOS short circuit simulation, a short between nodes should be a proper resistor between nodes instead of zero resistance [1], especially in an integrated circuit [2][3]. Therefore, it is advantageous to study testing by relating the system specifications to details of the layout and process. It is necessary to investigate correlations between fault models and physical failures. Based on the probability of the occurrence of physical failures and the fault behaviours caused by such failures, a realistic fault list can be generated and the fault models can then be built. Fantini and Morandi have presented a review on failure modes and mechanisms for very large scale integration (VLSI) ICs [4]. Failure mechanisms for electronic components are presented briefly in the following section.

2.2 Failure modes in electronic components

A failure mode is the effect by which a failure is observed, while a failure mechanism is the chemical, physical, or metallurgical process, which leads to component failure [5]. In electronic components, there exist different failure modes such as open circuit, short circuit, degraded performance and functional failures. Degradation faults depend mainly on variations of certain parameters of the components used in a circuit from its nominal values. This may be due to manufacturing defects, process variations, change in the environment or ambient temperature and/or wear out due to aging. Functional faults, on the other hand, are based on the fact that a circuit may continue to function, but some of its performance specifications may lie outside their acceptable ranges. For example, an amplifier may continue to amplify with a very low gain. Birolini [6] has summarised the relative occurrence of failure modes in some electronic components, which are shown in Table 2-I.

Table 2-I shows that most physical failures are open and short faults, which are comparatively easier to detect than degradation and functional faults. For example, an amplifier may continue to amplify with a very low gain. In printed circuit boards (PCBs), approximately 75% of faults occur at assembly, only 20% are component faults, and 5% are PCB faults [7].

An important application of Table 2-I is to calculate test coverage and yield estimation. For instance, if the open fault for a fixed resistor can be detected, 90% test coverage for that resistor is estimated. Further, faults in electronic components can be classified into following three groups with respect to their origin [8]:

1. *Electrical stress failures:* Being an event dependent failure mechanism, electrical stress is a continuous source of device defects over product lifetime. It is most often caused by improper handling.
2. *Intrinsic failures:* The group of intrinsic failures subsumes all crystal related defects. Since such defects depend very much on the maturity of the manufacturing process, they most often lead to yield loss or infant mortality, rarely to wear-out effects (gate-oxide wear-out and wear-out due to surface charge effects or ionic contamination have been observed). Type and manifestation of intrinsic failures are determined by technology: Gate-oxide defects are specific to metal-oxide semiconductor (MOS) devices by their nature, while current gain shifts are a typical bipolar device defect manifestation. Performance degradation is a long-term effect of intrinsic failures.
3. *Extrinsic failures:* Extrinsic failures comprise all defects related to interconnection, passivation and packaging. They can be classified into three categories with respect to the time of defect manifestation:

- severe process deficiencies resulting in easy-to-detect errors (e.g., open bonding),
- wear-out effects affecting long term reliability (e.g., moisture-related failures) and
- radiation-related errors continuously occurring over product lifetime.

Table 2-I: Relative occurrence of failure modes in some electronic components [6].

components	short %	open %	degradation %	functional %
digital, bipolar ICs	30	30	10	30
digital MOS ICs	20	10	30	40
linear ICs	30	10	10	50
bipolar transistors	70	20	10	--
field-effect transistors	80	10	10	--
diodes, general purpose	70	30	--	--
diodes, sneer	60	30	10	--
diodes, HF	80	20	--	--
SCRs	20	20	60	--
opto-electronic devices	10	50	40	--
resistors, fixed	90	10	--	--
resistors, variable	60	20	20	--
capacitors, foil	80	10	10	--
capacitors, metal foil	40	60	--	--
capacitors, ceramic	50	40	10	--
capacitors, tantalum, dry	60	20	20	--
capacitors, aluminium, wet	20	10	70	--
coils	10	30	--	60
relays	15	15	--	70
crystals	--	80	20	--

The probability of wear-out defects is strongly influenced by the package type. An appreciable percentage of field failures due to packaging can be traced to moisture in the package. The widely used plastic package exhibits the worst quality. Due to their low power dissipation, CMOS devices are more susceptible to corrosion than other devices. The order of importance of the failure mechanisms further depends on parameters like device size,

maturity of the technology, and extent and effectiveness of the screening applied after production. With a proportion of 58% [8], electrical stress induced defects play a dominant role in the field failures. A vast majority of failure mechanisms is extremely temperature dependent. High temperature or temperature cycling, lead to significant increase in failure rate, the same applies for high supply voltage also. Table 2-II gives typical examples for each of these groups, for a detailed discussion, please refer to [8].

Table 2-II: Global classification of component failures [8].

failure group	relevant parameters	time distribution of failures
electrical stress	handling	continuous
intrinsic	technology	predominantly infant but also wear-out
	process	yield loss
extrinsic	packaging	wear-out, rarely infant
	radiation	continuous

An effective fault model is a fundamental issue for a successful analog test and diagnosis strategy. In the following section, an attempt has been made to provide an outline of analog fault modelling.

2.3 Analog fault modelling

The fault list is the set of all modelled faults and the test generated by the test process should detect all modelled faults. Realistic analog fault models can be achieved by knowing the behaviour of the circuit. In general, an analog IC under test can have the following three outcomes:

1. *Catastrophic (hard) failure:* The circuit is not functioning at all.
2. *Unacceptable performance degradation:* In this case, the circuit is still functioning, but some of its performance specifications lie outside their acceptable range. Performance degradation is usually referred to as a *soft* failure.
3. *Acceptable performance:* The circuit is functioning and all its performance parameters are within their specification ranges. In this case, the circuit is said to be *correct.*

From above, faults in analog ICs are generally classified in to the following two categories [9]:

- *Catastrophic (hard) faults:* Catastrophic faults are all those changes to the circuit that cause the circuit to fail catastrophically. These faults include shorts, opens or large variations of a design parameter

like forward beta (β) in bipolar junction transistors (BJTs) and width and length of MOS field effect transistors (MOSFETs). Catastrophic faults are caused by major structural deformations or extreme out-of-range parameters and lead to failures that manifest themselves in a completely malfunctioning circuit. Electro-migration and particle contamination phenomena occurring in the conducting and metallisation layers are the major causes of opens and bridging shorts.

- *Parametric (soft) faults:* Parametric faults are those changes that cause performance degradation of the circuit. These faults are due to the process fluctuations. These faults involve parameters' deviations from their nominal value that can consequently quit their tolerance band. Parametric faults are due to out-of-specification parameter deviations and so depend on the acceptability band defined by tolerances of process parameters.

As analog faults are continuous in mode they can take an infinite number of values and so, the only difference between catastrophic and parametric faults depend on the concept of "totally malfunctioning circuit". In addition, faults considered catastrophic at one description level may become parametric at a higher one. Further, a good knowledge of the probability of occurrence of all possible defects is necessary for actual fault coverage estimation by a test methodology. From the perspective of physical failure mechanisms, changes to a circuit comes from a wide range of sources [10] such as manufacturing defects, process variations, circuit and environmental parasitic, changes in the environment or ambient temperature, and design errors/non-robustness.

Numerous techniques based on the catastrophic and/or parametric fault models with emphasis on either stimuli design (i.e., test generation) [11][12][13][14][15][16][17][18][19], or response analysis (i.e., signature analysis for deriving the acceptance region) [20][21][22][23] has been proposed. The works in [14][17][18][19] address the test generation problem in the frequency domain for linear time-invariant (LTI) circuits. Sinusoidal stimuli with specific frequency, which maximises the output difference between the faulty and fault-free circuit are selected as the input stimuli. Specifically parametric deviation that could possibly mask the faults is considered in the selection of frequency [19]. A symbol based approach for deriving the test frequency is demonstrated in [17]. Methods of test generation in time domain are addressed in [12][13][15][16] which derive static or dynamic time domain test stimuli. Elsewhere, test generation is formulated as a linear [15], quadratic [13] or dynamic [16] programming problem to maximise the output difference. These time domain test generation techniques usually can be applied to both linear and non-linear circuits. Techniques using the

tolerance range of device parameters for analog circuit fault detection are proposed in [20][21][22]. Fault-model based techniques for AMS testing of [24][25][26] includes DC voltage/current and pseudorandom excitation techniques. In the DC technique, the DC output voltages/currents are used as signatures. Modelling of analog and mixed-signal ICs for testing and fault diagnosis using standard test stimuli generated for digital ICs have been reported in [27][28][29].

In the above studies, the faults are modelled mostly as open, short, and variable component values. However, component value changes are usually significant in these failure modes. As a result, a faulty value with a value ten times larger or ten times smaller is a reasonable assumption in generating the fault list. Open and short faults are only the extreme cases of these two. Therefore, if ten times larger or ten times smaller faults can be covered, the open and short faults can be detected also. In IC models, short and open should be considered as resistive values according to the technology and process [30]. The information provided in the literatures can be used for making test decisions, creating fault models, generating fault lists, and calculating fault coverage in fault simulation. A comprehensive structured approach for testing and fault diagnosis of AMS circuits and systems have not yet materialised.

The basic problem with analog IC fault diagnosis is the absence of efficient fault models [31], component tolerances and non-linearities. It is difficult to arrive at a general fault model like the stuck-at models for the digital circuits. As described above faults in analog ICs can be classified into two categories:

catastrophic faults or hard faults
parametric faults or soft faults

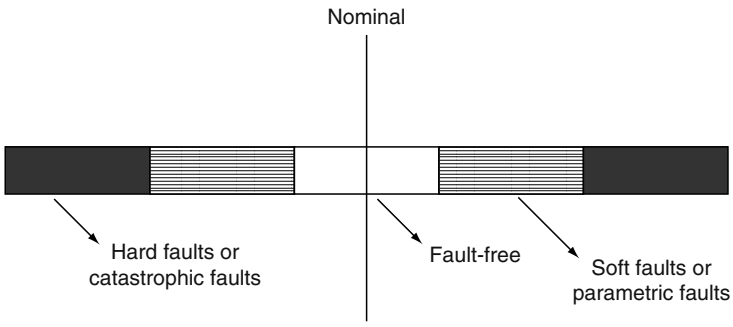

Figure 2.1: Taxonomy of faults.

Therefore the taxonomy of analog faults can be represented as shown in Figure 2.1. There is a region of acceptable behaviour around nominal range. Beyond this region, there is circuit performance that does not meet design specification, but does not cause complete circuit failure. Finally there are faults that render the circuit inoperable. Since both hard faults and soft faults can take on infinitely many varieties, there are infinitely many analog faults. Consequently, we must choose a subset of faults, which will lead to the best possible fault list.

Since 80-to-90 percent of analog faults involve shorted and open resistors, capacitors, diodes and transistors [6], in this study we have chosen the fault models of various devices as shown in Figure 2.2. Open faults are hard faults in which the component terminals are out of contact with the rest of the circuit creating a high resistance at the incidence of fault in the circuit. Addition of a high resistance in series (e.g., RS ≥ 1 MΩ) with the component (e.g., resistor, capacitor or diode) can simulate the open faults. Short faults, on the other hand, are a short between terminals of the component (effectively shorting out the component from the circuit). A small resistor in parallel (e.g., RP ≤ 1 Ω) with the component can simulate this type of fault for resistors, capacitors and diodes.

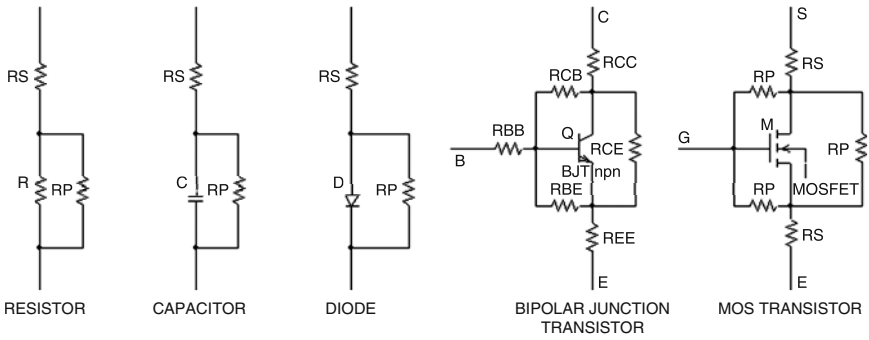

Figure 2.2: Fault models of resistor, capacitor, diode and transistor.

The BJT can have three open faults (at the base, collector and emitter terminals) and three short faults (between base-emitter, collector-base and collector-emitter). These open and short faults are emulated in the same manner using three series resistors RBB, RCC and REE for the open faults and three parallel resistors RBE, RCB and RCE respectively as shown in Figure 2.2. In addition, the BJT has two extreme out-of-range parametric faults for the value of beta (β). A MOSFET has five hard faults: two stuck-open faults at the source and drain, and three stuck-short faults between

source-drain, drain-gate and gate-source [32]. These stuck-open faults can be emulated using a high resistance RS in series and the stuck-short faults can be emulated using a small resistance RP between the terminals using the fault model as shown in Figure 2.2.

With this set of fault models we obtain a standard set of faults. The total number of catastrophic faults in a BJT integrated circuit can be

$$N_{CF} = 2(R + C + D) + 8B \tag{2.1}$$

and that in a MOS integrated circuit can be

$$N_{CF} = 2(R + C + D) + 5M \tag{2.2}$$

where R = number of resistors, C = number of capacitors, D = number of diodes, B = number of BJTs, and M = number of MOSFETs.

In practical circuits, the soft faults are the most difficult to model and test. The first problem in the testing of soft faults in analog ICs is to decide on what kind of circuit component deviations from nominal should be considered faulty. Deciding on the tolerance is a major hurdle. The enormous fault list is rendered manageable by quantising the possible values that a circuit under fault can take. The fault free category includes all the values lying in the range $N \pm \sigma$, where N is the nominal value and σ is the standard deviation from the nominal value. A circuit component having any value in this range is considered fault-free. If it maps to some value outside this nominal range, it is considered faulty. Moreover it could be faulty either above or below the tolerance. While simulating the bipolar analog ICs for fault conditions, these soft faults can be modelled using a reduced set of SPICE parameters like forward and reverse β, junction capacitance, transport saturation current, forward Early voltage, forward and reverse transit time, etc. of the devices. Similarly, for simulating the MOS analog ICs for fault conditions, these soft faults can be modelled using parameters like channel length, channel width, saturation current, threshold voltage, oxide thickness, etc. of the devices.

2.4 Approximation modelling of analog integrated circuits

As described later in Chapter 4, one of the important concepts of fault diagnosis in analog ICs is the use of model-based observer scheme. The development of approximation models based on the physical information and data of the analog IC under test is the foremost goal of such a fault

diagnosis methodology. Approximation models that can be used for modelling of failures in any dynamical system may be any one of the various types of mathematical models available in the literature [33]. Some important types of approximation models are given below:

1. *Polynomials:* Polynomial approximation is the most extensively studied approximation method. The class of polynomial functions of degree *n* is given by

$$\hat{f}_n(z;\hat{\theta}) := \left\{ \sum_{i=0}^{n} \hat{\theta}_i z^i : \hat{\theta}_i \in R, \hat{\theta}_n \neq 0 \right\} \tag{2.3}$$

   Polynomials are linearly parameterised approximators and according to the well-known Weierstrass theorem [33], for any function $f \in C[D]$ and any $\varepsilon > 0$, there exist a polynomial $p \in \hat{f}_n$ (for *n* arbitrarily large) such that $\sup_{z \in D} | f(z) - p(z) | \leq \varepsilon$. In the special case of *n=1*, the polynomial expansion reduces to a linear system, which constitutes the best-developed part of system theory.
2. *Rational functions:* Another type of approximation method is the rational function approximation. In this case

$$\hat{f}_{n,m}(z;\hat{\theta},\hat{\vartheta}) := \left\{ \frac{\sum_{i=0}^{n} \hat{\theta}_i z^i}{\sum_{i=0}^{m} \hat{\vartheta}_i z^i} : \hat{\theta}_i, \hat{\vartheta}_i \in R \right\} \tag{2.4}$$

   with the restriction that the zeros of the denominator polynomial are outside the approximation region. In general, rational functions have greater approximation power than polynomial functions, in the sense that with the same number of parameters one is able to obtain better approximation accuracy [33]. Rational functions are nonlinearly parameterised approximators.
3. *Spline functions:* Spline functions are examples of piecewise polynomial approximators [34]. The main idea behind spline functions is the partition of the approximation region into a finite number of sub-regions via the use of *knots.* In each sub-region a polynomial of degree at most *n* is used, with the additional requirement that the overall function is (*n-1*) times differentiable. The most popular type of spline functions is *cubic splines* where *n=3*, i.e., cubic polynomial pieces that are joined so that the overall function is twice differentiable. Spline functions with fixed knots are

linearly parameterised approximators; however, spline functions with variable knots become nonlinearly parameterised approximators.

4. *Artificial neural networks (ANNs):* ANNs are approximation methods based on models of biological signal activity [35]. Although various ANN models have been proposed, by far the most popular is the class of multi-layer ANNs with sigmoid-type activation function. In the case of a two layer ANN

$$\hat{f}_n(z;\hat{\theta},\hat{\vartheta},\hat{\varphi}) := \left\{ \sum_{i=1}^{n} \hat{\theta}_i \sigma(\hat{\vartheta}_i z + \hat{\varphi}_i) : \hat{\theta}_i, \hat{\vartheta}_i, \hat{\varphi}_i \in R \right\} \tag{2.5}$$

where, $\sigma(\bullet)$ is the sigmoid activation function. Theoretical works by several researchers have shown that such networks can uniformly approximate any function $f \in C[D]$ to any degree of accuracy (universal approximation), provided n is sufficiently large, or equivalently the network has sufficiently large number of neurons. Multi-layer ANNs are nonlinearly parameterised approximators.

5. *Radial-bias-function networks:* Another class of neural networks that has attracted considerable attention is the radial-bias-function (RBF) network model. The output of the RBF network is of the form

$$\hat{f}_n(z;\hat{\theta}) := \left\{ \sum_{i=1}^{n} \hat{\theta}_i \omega_i(z) : \hat{\theta}_i \in R \right\} \tag{2.6}$$

where, ω_i is the output of the i[th] basis function. The Gaussian function $\omega_i(z) := \exp(-|z - c_i|^2 / \sigma_i^2)$, where c_i and σ_i are the i[th] centre and width respectively, is usually chosen as the basis function. RBF networks are also capable of universal approximation. In many respects, the approximation properties of RBF networks are similar to those of spline functions. For example, if the centre and width are kept fixed then the RBF networks are linearly parameterised approximators; if they are allowed to vary then RBF networks become nonlinearly parameterised approximators.

6. *Adaptive fuzzy systems:* The fuzzy logic paradigm [35] provides another type of approximator. Fuzzy systems approximate functions by covering their graphs with fuzzy patches or fuzzy rules of the form "if antecedent conditions hold, then consequent conditions hold". The approximation increases in accuracy as the fuzzy patches increase in number and decrease in size. In adaptive fuzzy systems

each fuzzy rule is weighted by adjustable parameters or weights. Fuzzy systems offer the possibility of using linguistic information, based for example on common sense or experts' knowledge, for control of systems where a mathematical model is hard to determine.

To simplify the notations in the above approximation methods, the case of single-variable functions (z is a scalar) are considered. The above list of approximators, although not complete, includes many of the approximation methods used for modelling of dynamical systems. The first three of the approximators described above are based on classical approximation methods while the rest have been proposed in the context of "intelligent control".

The preceding discussion indicates that ANNs represent one class of on-line approximators. Investigations comparing neural networks with other approximation models are still at a preliminary stage; however, from a system engineering perspective, ANNs possess several properties that make them appropriate for approximation of unknown systems, in the context of fault diagnosis. Some of these properties are:

- Massive parallelism,
- Fault tolerance,
- Possibility of analog hardware implementation,
- Convenient adaptation capabilities and
- Good generalisation features.

Furthermore, ANNs have received a great deal of research interest in the past several years and two tutorial articles [36][37] describe the various types of ANNs that are mostly used. ANNs lead to solutions of problems in pattern recognition, associative memory, database retrieval and process fault detection and identification even in the following environment:

- Poorly defined models
- Noisy inputs
- Nonlinear systems

The choice of network architecture is growing. Hsu et al. [38] outlines a comparison of five different ANN architectures and have shown that the backward error propagation (BEP) algorithm provides the best results for the pattern classification task. Many other workers have also had success using the BEP network [39][40][41][42][43][44][45]. These researchers and others provide sufficient confidence in the advantages of the use of ANNs in fault diagnosis of analog ICs. An overview of the ANN is presented in Appendix A.

2.5 Summary

This chapter has presented fault and fault modelling in general and that of analog IC in particular. Section 2.1 gave an introduction to the subject. The definition of the faults has been discussed in this section. This section also presented the fault mechanism.

Section 2.2 discussed the failure modes in electronic components. A clear understanding of failure modes is important to avoid any confusion in the development of analog fault modelling.

Analog fault modelling was presented in section 2.3. Both the catastrophic and parametric faults of BJT and MOSFET have been considered. This section also discussed the different techniques of fault modelling. Fault model of resistor, capacitor, diode and transistors are covered here.

Section 2.4 discussed some of the important approximation modelling of the analog integrated circuits.

Before beginning the study of the following chapters the reader may wish to study the appendix A that presents an overview of the ANN. It covers model of an artificial neuron, the activation function and the structure of an ANN. A good understanding of the ANN will provide a firm foundation for later chapters and subject materials.

Exercises

2.1. What are the different types of failure possible in an electronic component? How do the layout of an integrated circuit and its packages affect failure of the device? Why does the CMOS short circuit simulation use a resistor instead of zero resistance?

2.2. Count the possible number of catastrophic faults for the circuit of Fig. 2.3

2.3. Show that the interest compounded annually over a particular number of years on a principal could be expressed as a polynomial of the interest rate per annum, r. The cumulative increase in the principal, R, could be expressed with an r^0 component included.

2.4. The following data has to be fitted in with a quartic polynomial where the augmented principal is a polynomial function of the interest rate:

Interest rate per annum (r)	3	4	5	6	7	8	9	10
Augmented Principal (R)	108	113	122	126	131	136	141	146

Some uncertainty is added to the data because of the rounding off of R. Use least squares (LS) method to get the polynomial coefficients.

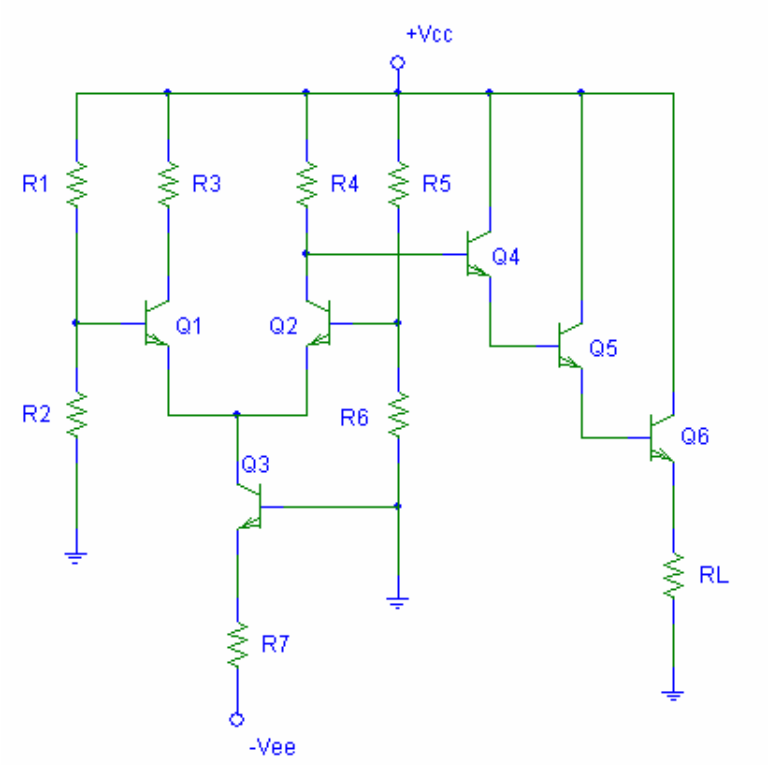

Figure 2.3: ***Circuit diagram for Exercise 2.2.***

2.5. Could the above data be fitted by a rational function (equation 2.4 of section 2.4) having less number of coefficients than those of the polynomial approximation? [Try LS fit again.]

2.6. (a) Try to approximate the function $f(x) = x^4$ on the interval [0, 1] with only one polynomial piece. [A possible cubic spline function is $2x^3 - x^2$.]

(b) Again approximate $f(x) = x^4$ on [0, 1], but this time use two polynomial pieces so that x = [0, ½, 1], that is, use cubic splines with multiple (two) knots. Is there any improvement in the accuracy of representation?

2.7. Plot the function given in problem 2.4. Create an artificial neural network (ANN) with one input layer, one output layer and a hidden layer to approximate the above function. Choose proper weights for

the links and biases for the neurons using a training set and back propagation algorithm (BEP). [Use MATLAB library routine for the purpose.]

2.8. Given below are 21 inputs P and associated target points T:
P = (–1, 0.1, +1)
T = (–0.9602, –0.5770, –0.0729, –0.3771, +0.6405, +0.6600, +0.4609, +0.1336, –0.2013, –0.4344, –0.5000, –0. 3930, –0.1647, +0.0988, +0.3072, +0.3960, +0.3449, +0.1816. –0.0312, –0.2189, –0.3201)
Define a suitable radial basis function (RBF) which could be used to fit the above target points. Now create a radial basis network which will approximate the function defined by P and T.

2.9. Try fitting in linguistic variables to describe the data given in problems 2.6 and 2.8 and define corresponding rule bases to explain the behaviour of the data.

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